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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,533	02/27/2002	Hiroshi Hashimoto	020244	6400

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,533	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *16-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-5, 7-12, 14-15 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6251728 to Patelmo in view of Applicant Admitted Prior Art (APA).

Regarding claims 1, Patelmo discloses a semiconductor integrated circuit (IC) device fig. 23, comprising: a substrate 2, column line 40, a nonvolatile memory device

EEPROM 72, column 7 line 10, formed in a memory cell region of substrate 2 and having a multilayer gate electrode structure comprising a tunnel insulating film 26, column 3 line 55, covering substrate 2 and floating gate electrode 27b, column 6 line 48, formed on the tunnel insulating film 26 and having a side wall surfaces covered with a protection insulating film formed of an oxide 31; and a semiconductor device 71, column 7 line 10, formed in a device region of substrate 2, the semiconductor device comprising a gate insulating film 34, column 5 line 28, covering substrate 2 and gate electrode 43d, column 7 line 37, formed on the gate insulating film 34, wherein the bird's beak structure is formed at an interface of the tunnel insulating film 26 and the floating gate electrode 27b along the interface from the sidewall faces of the floating gate electrode 27b, the gate insulating film 34 is interposed between substrate 2 and the gate electrode 43d have a substantially uniform thickness at the region under the gate electrode, fig. 23.

But, Patelmo does not discloses a semiconductor IC device wherein the bird's beak structure is formed in accordance with a film thickness of the protection insulating film of 5-10 nm.

However, APA discloses the flash memory cell wherein the bird's beak structure is formed in accordance with a film thickness of the protection insulating film 18, fig. 8A, of 5-10 nm, specification page 13 lines 5-10. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the insulating film teaching of APA with Patelmo's device, because it would have protected the gate structure.

The process limitations "the thermal" and "the bird's beak structure under floating gate electrode is formed simultaneously with the formation of protection insulating film" in claim 1, does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985). A 'simultaneously formed' does not create a distinctive or different structure from the Patelmo's device.

Regarding claims 2-3, 12, Patelmo discloses the IC device wherein the multiplayer gate electrode structure further comprises an insulating film 31, column 4 line 14, formed on the floating gate electrode 27b and a control gate electrode 43b, column 7 line 22, formed on the insulated film 31, wherein each of the gate electrode 43d and control gate electrode 27b comprises doped polysilicon, column 3 line 58 and column 4 line 60.

Regarding claim 4-5, and 10-11, Patelmo discloses the IC device wherein the oxide film 31 connects the bird's beak structure, fig. 23, wherein the protection insulating film 66, column 7 line 8, continuously covers sidewall faces and a top surface of the multiple gate electrode structure, fig. 23.

Regarding claim 7, 14 Patelmo discloses the IC device having the tunnel oxide 26.

Regarding claim 9, Patelmo discloses a semiconductor integrated circuit device in fig. 23 comprising: a substrate 2, a nonvolatile memory device 72 formed in a memory cell region of said substrate 2, the nonvolatile memory device comprising: a first active region 22, fig. 23, covered with a tunnel insulating film 26; a second active region 65b, fig. 23, formed next to the first active region 23 and covered with an

insulating film 25, a control gate formed of an embedded diffusion region 30 formed in the first active region; a first gate electrode 27b extending on the tunnel insulating film 26 in the first active region 22 and forming a bridge between the first and second active regions to be capacitive-coupled via the insulating film 26 to the embedded diffusion region 30 in the first active region 22, the first gate electrode 27b having sidewall faces thereof covered with a protection insulating film formed of a oxide film 31; and a diffusion region 22, 65b, and 30 formed on each of sides of the first gate electrode 27b in the first active region; and a semiconductor device 71 formed in a device region of substrate 2, the semiconductor device 71 comprising a gate insulating film 34 covering substrate 2 and a second gate electrode 43d formed on the gate insulating film, fig. 23, wherein a bird's beak structure is formed of oxide film 26 at an interface of the tunnel insulating film 26 and the first gate electrode 27b, the bird's beak structure penetrating into the first gate electrode 37b along the interface of the first gate electrode 27b; and the gate insulating film 34 is interposed between said substrate 2 and the second gate electrode 43d to have a substantially uniform thickness at the region under the gate, fig. 23.

But, Patelmo does not discloses a semiconductor IC device wherein the bird's beak structure is formed in accordance with a film thickness of the protection insulating film of 5-10 nm.

However, APA discloses the flash memory cell wherein the bird's beak structure is formed in accordance with a film thickness of the protection insulating film 18, fig. 8A, of 5-10 nm, specification page 13 lines 5-10. At the time the

invention was made; it would have been obvious to one of ordinary skill in the art to use the insulating film teaching of APA with Patelmo's device, because it would have protected the gate structure.

The process limitations "the thermal" and "the bird's beak structure under floating gate electrode is formed simultaneously with the formation of protection insulating film" in claim 1, does not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985). A 'simultaneously formed' does not create a distinctive or different structure from the Patelmo's device.

Regarding claim 40, as discussed in the above claims 1-5, and 12, Patelmo and APA disclose all the limitations of claim 40.

Regarding to claims 8 and 15, Patelmo does not discloses the tunnel insulating film is a nitride oxide film.

However, APA discloses the IC device having the tunnel oxide 12, spec. page 2 or nitride, page 4. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the tunnel insulating material teaching of APA in the Patelmo's device, because such material substitution would have been considered a mere substitution of art-recognized equivalent values.

4. Claims 6, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6251728 to Patelmo and APA as applied to claims 1 and 9 above, and further in view of in view of US 6406959 to Prall et all.

Regarding claims 6, 13, Patelmo does not expressly disclose the semiconductor IC device wherein a SOI substrate is employed as substrate.

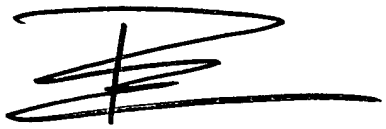
However, Prall reference discloses a flash memory device wherein the substrate 11 can be either silicon or SOI, column 4 line 15. At the time of the invention was made; it would have been obvious to one of ordinary skill in the art to replace the silicon substrate of APA with either Si or SOI substrate teaching of Prall, because such substrate substitution would have been considered a mere substitution of art-recognized equivalent values.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao X. Le
Patent Examiner
21 Jan. 2005